



FIG. 1

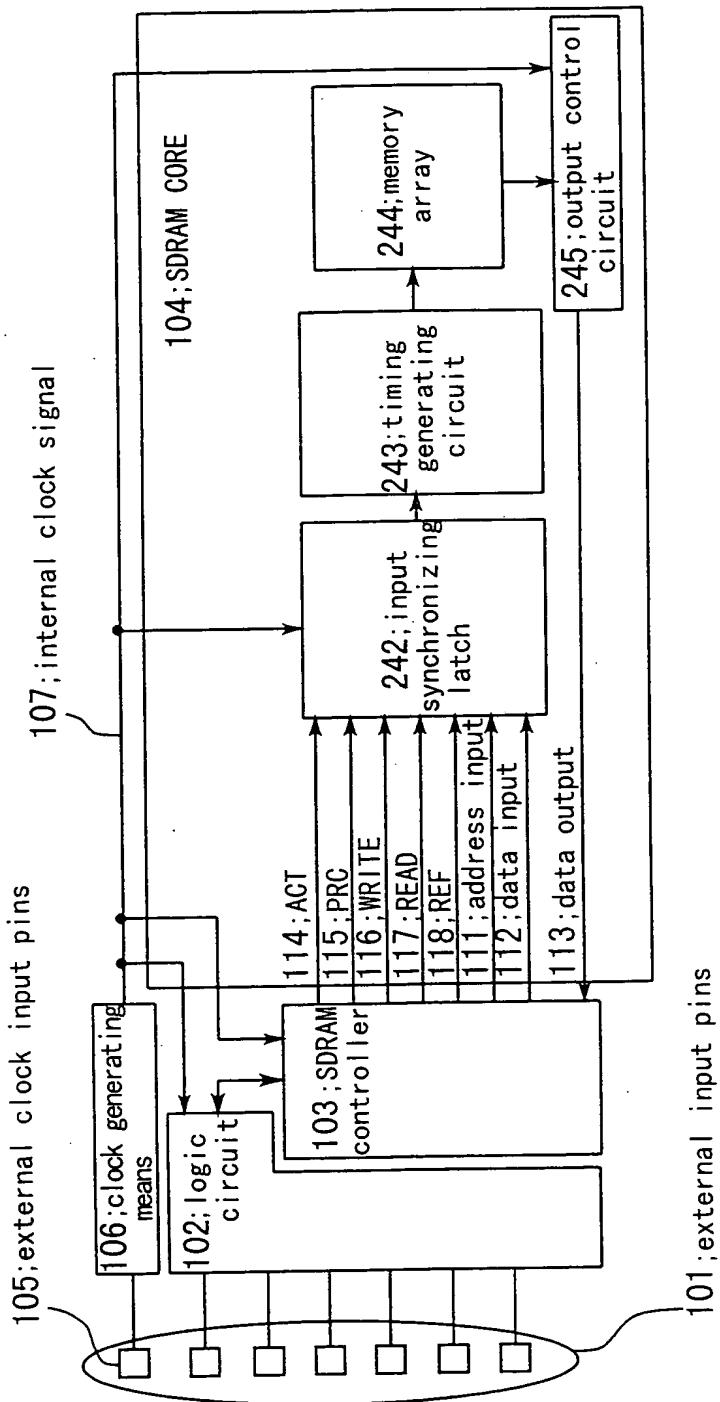




FIG. 2

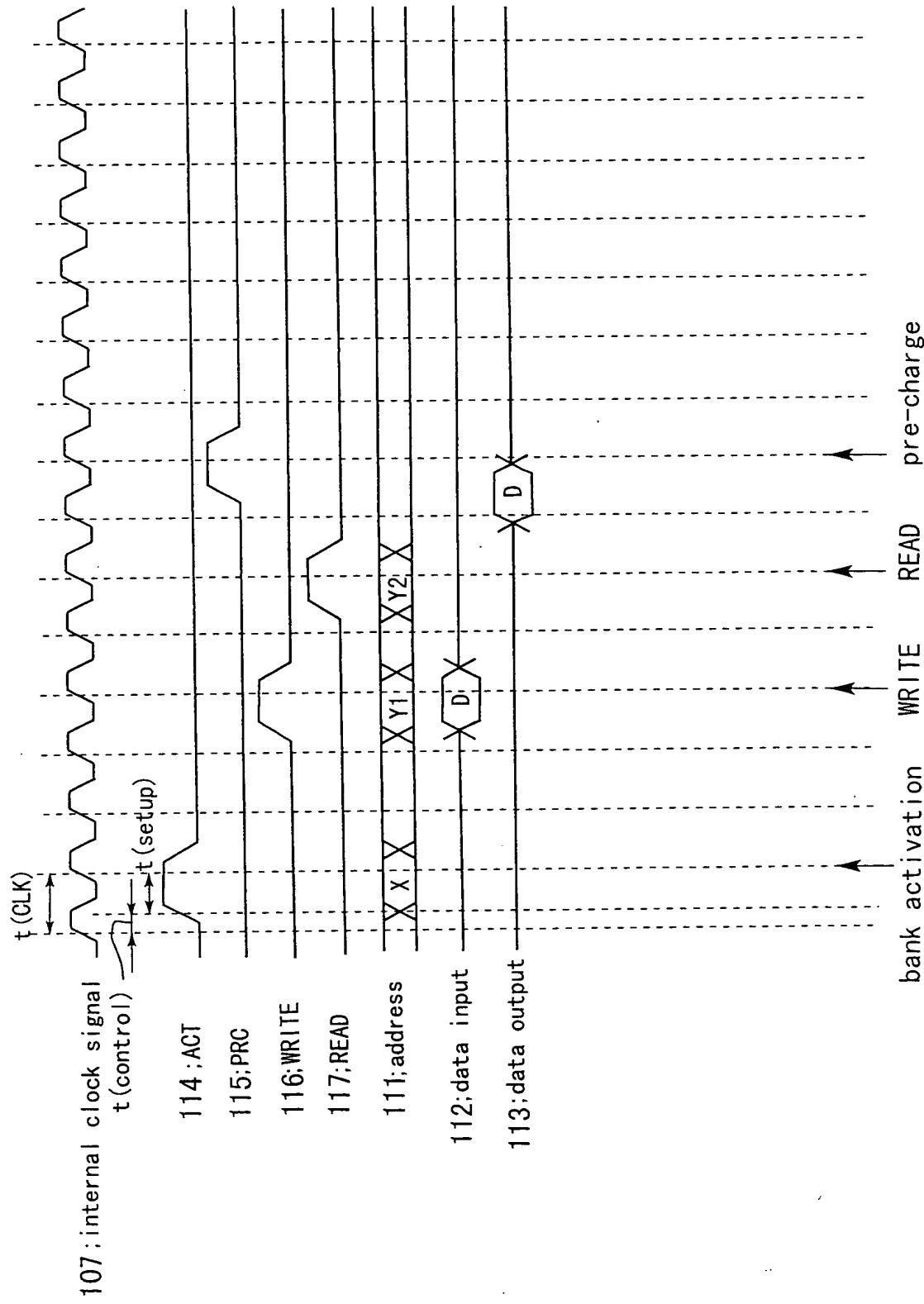




FIG. 3

105; external clock input pins

107; internal clock signal

106; clock generating means

102; logic circuit

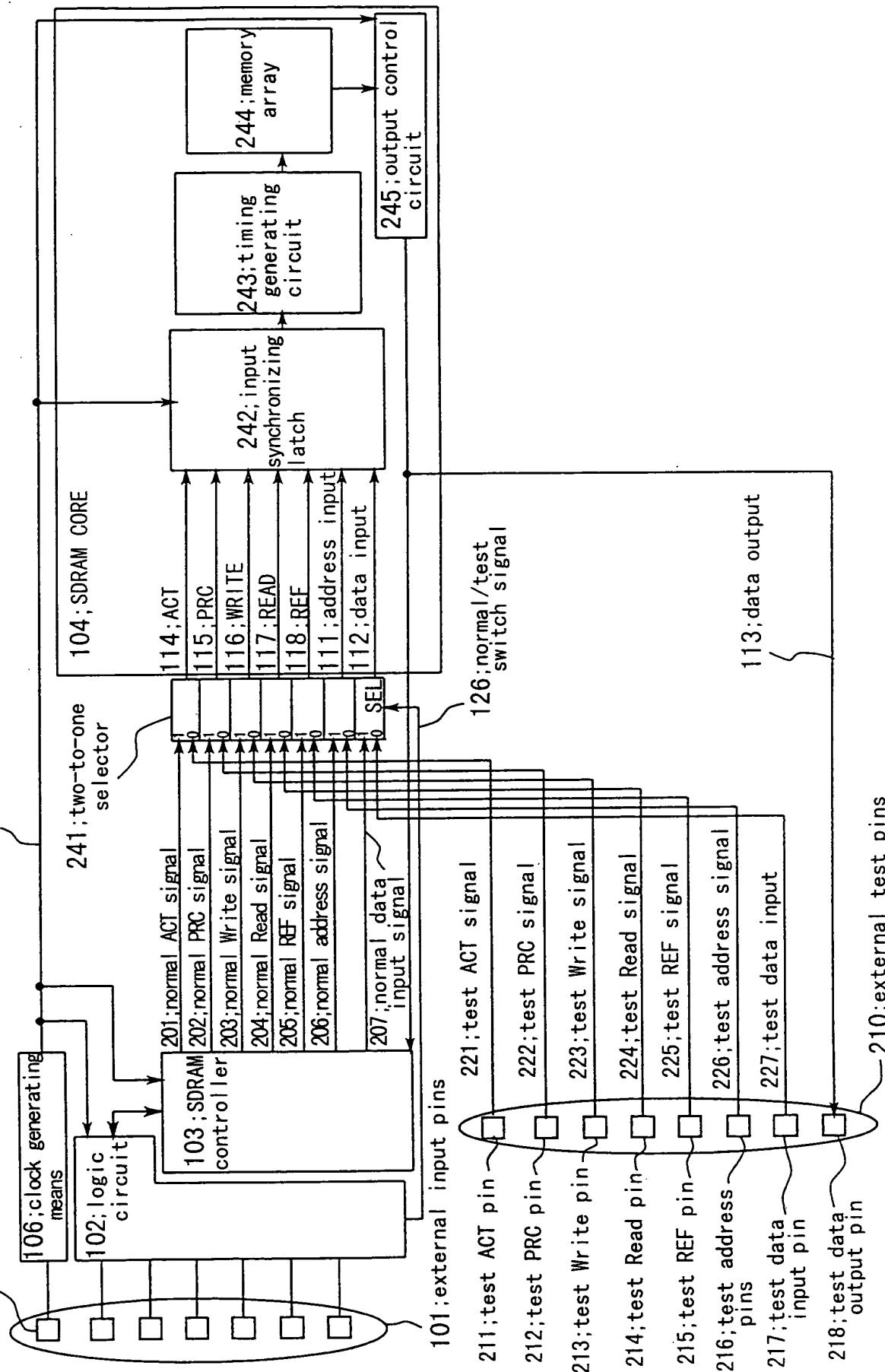




FIG. 4

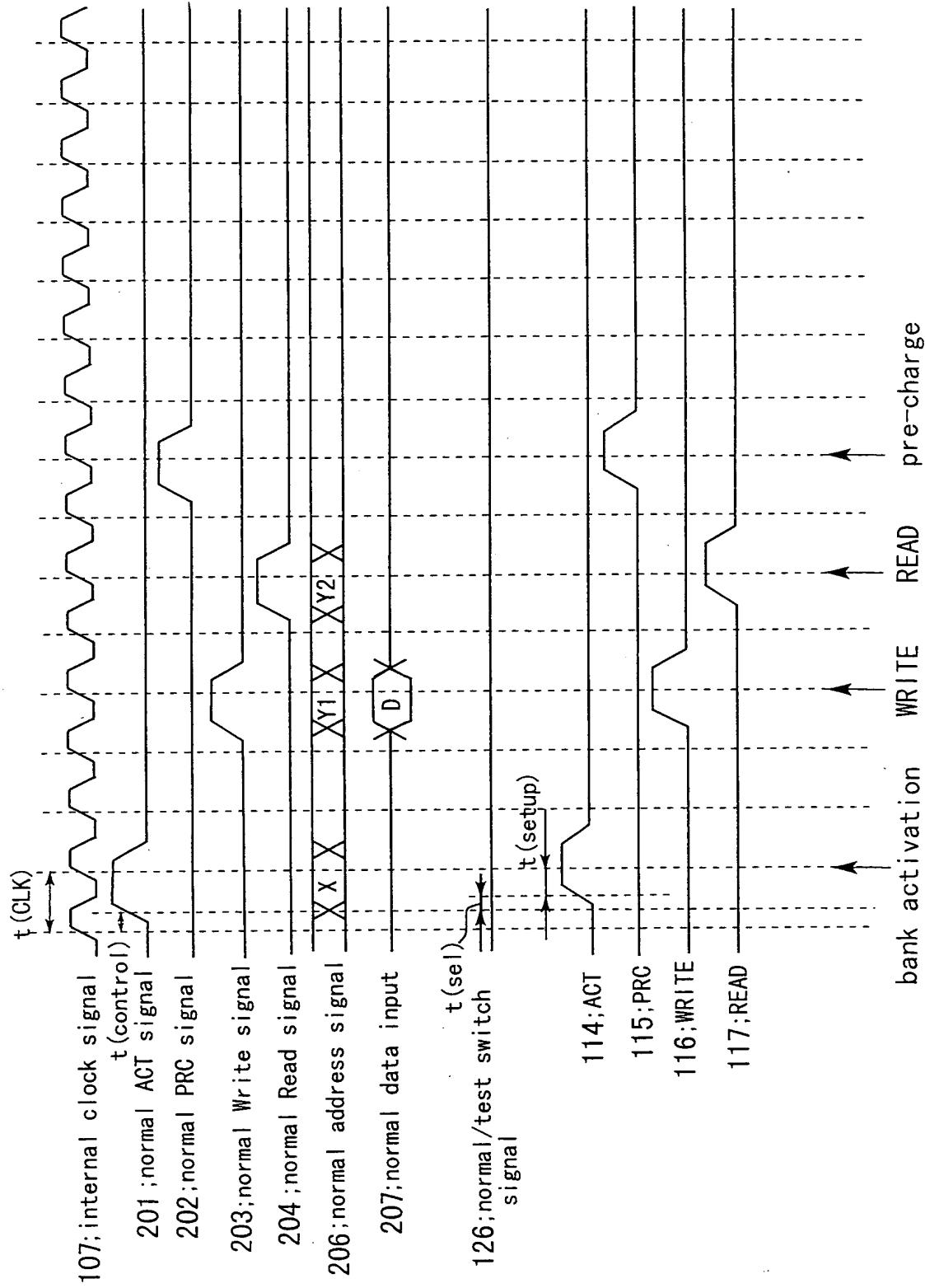




FIG. 5

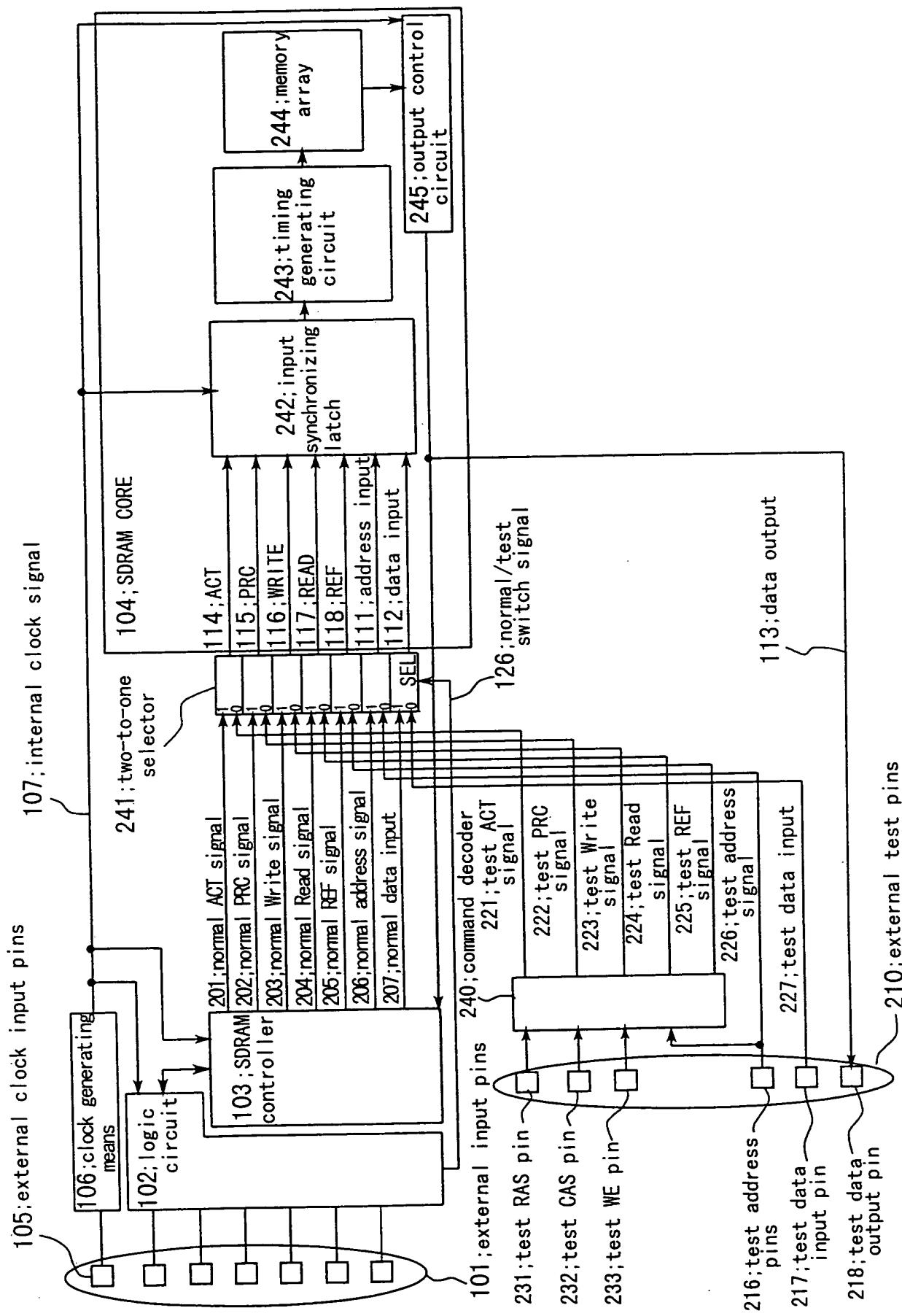


FIG. 6

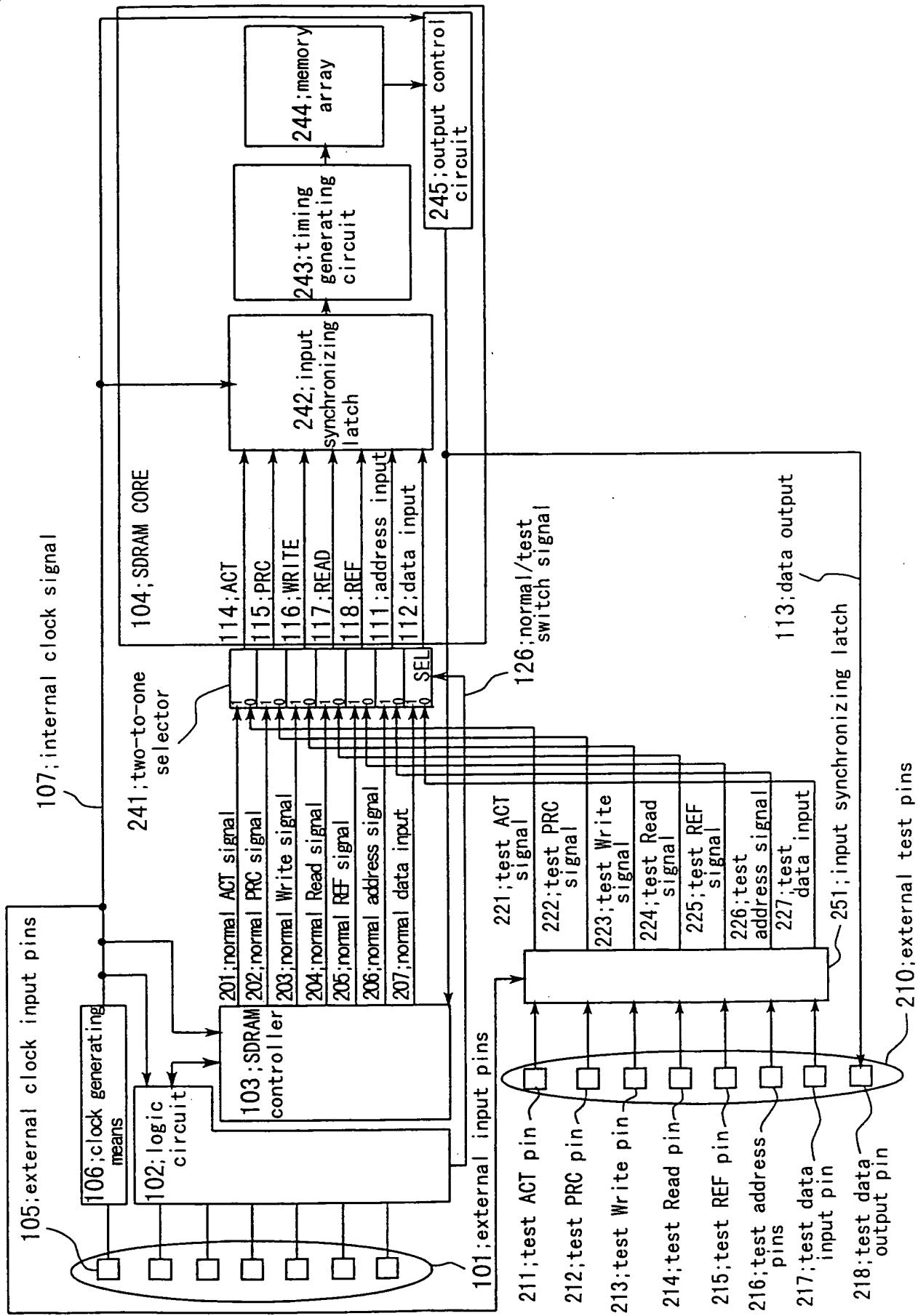




FIG. 7

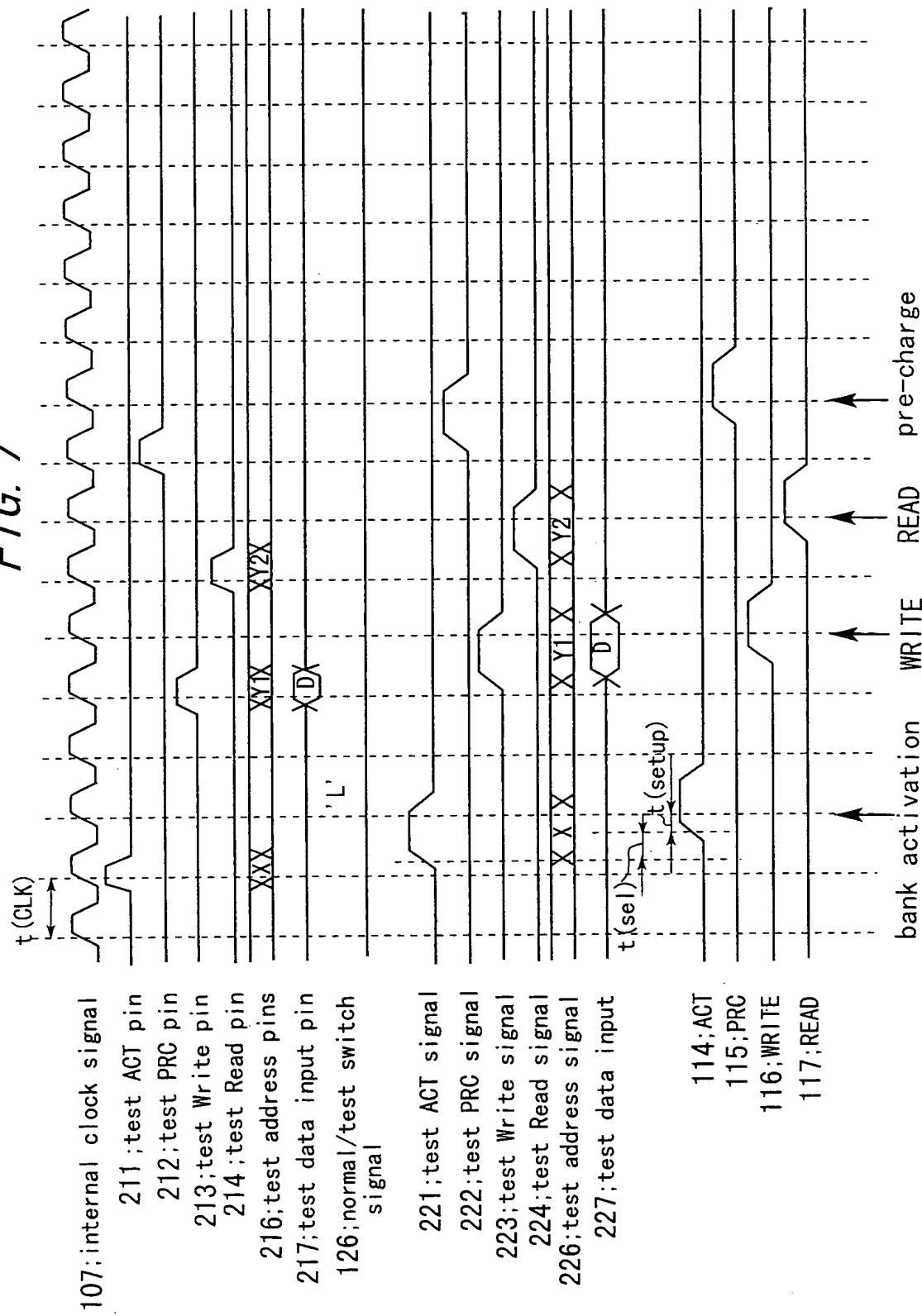




FIG. 8

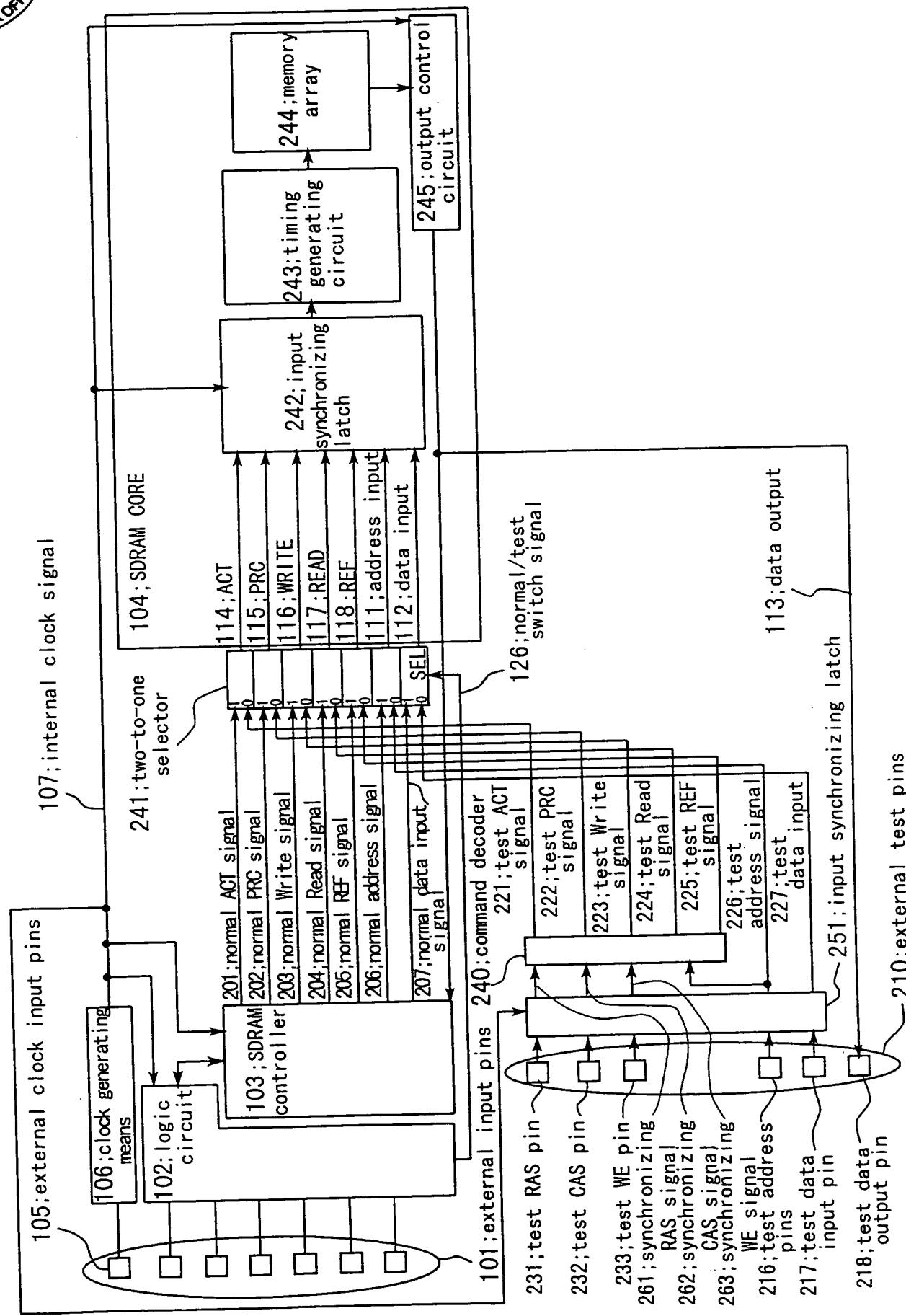




FIG. 9

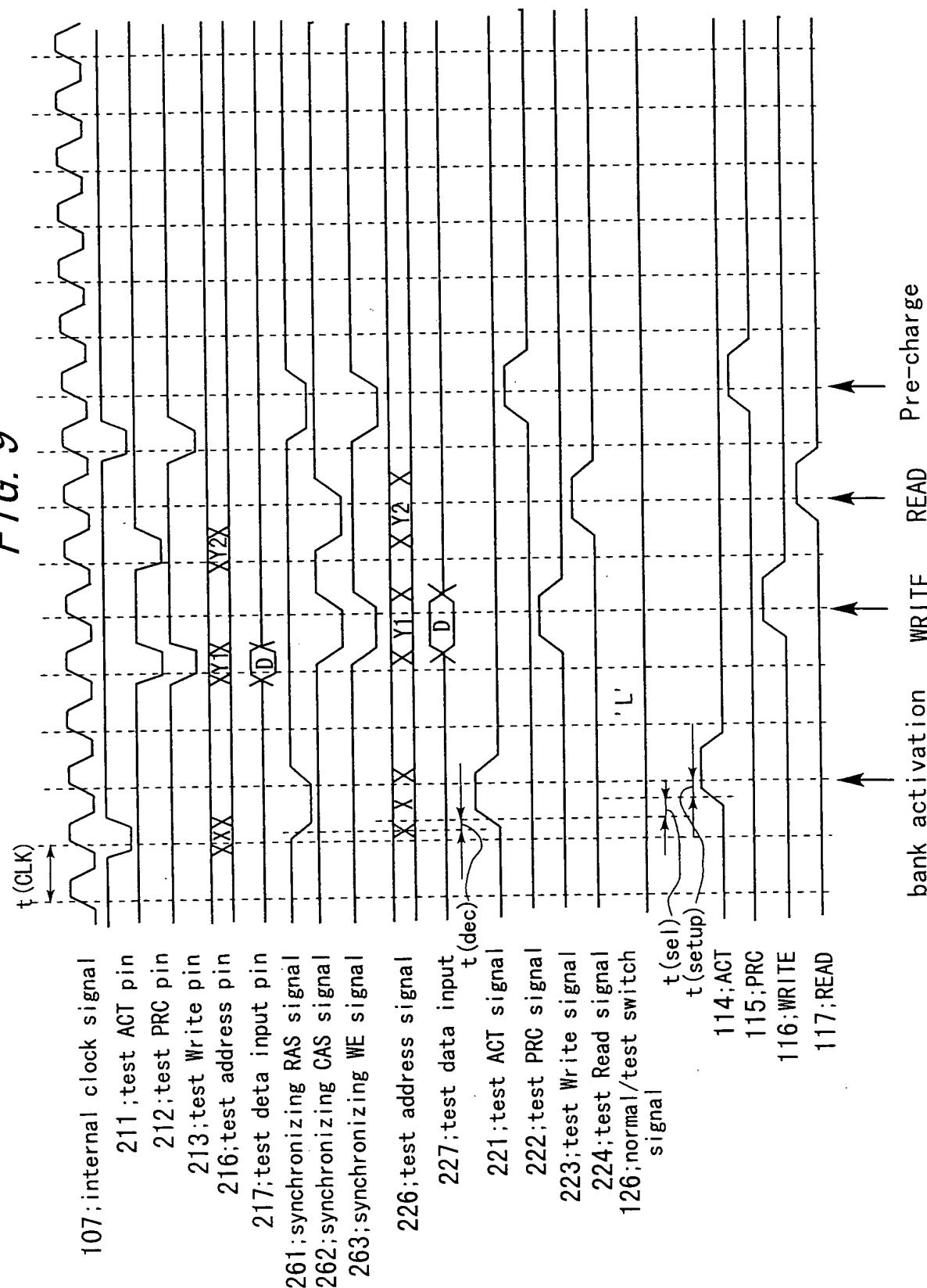




FIG. 10

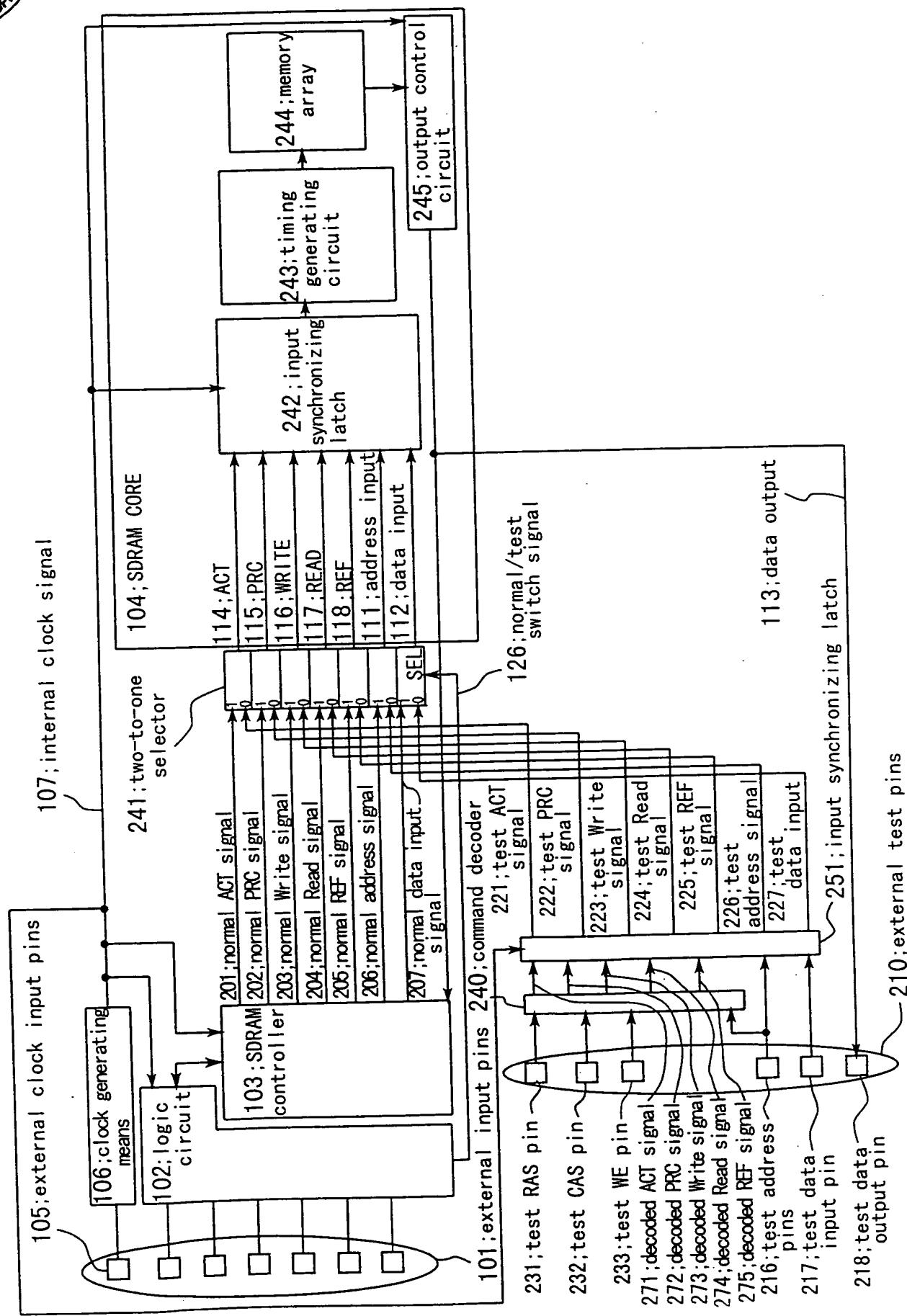




FIG. 11

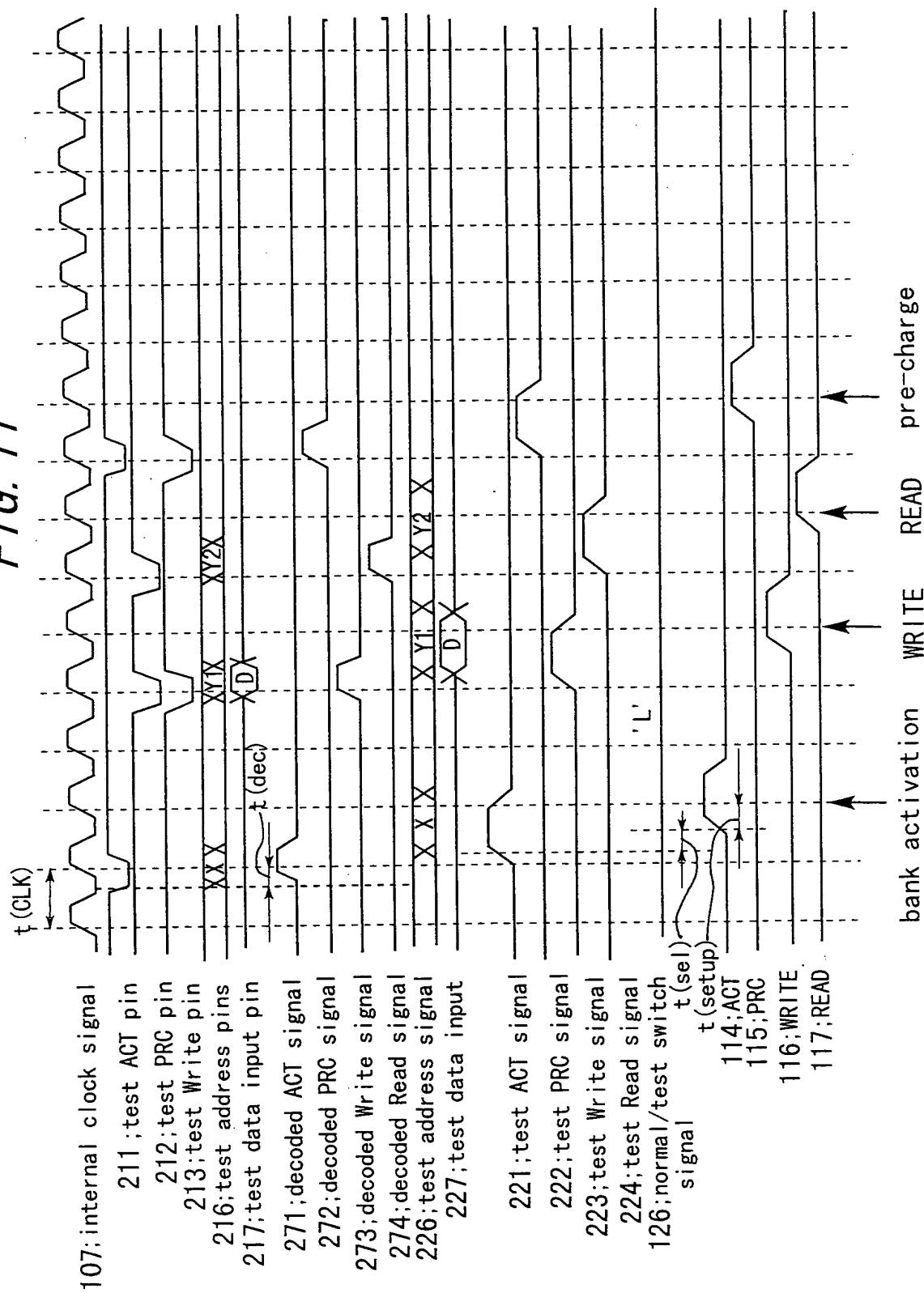
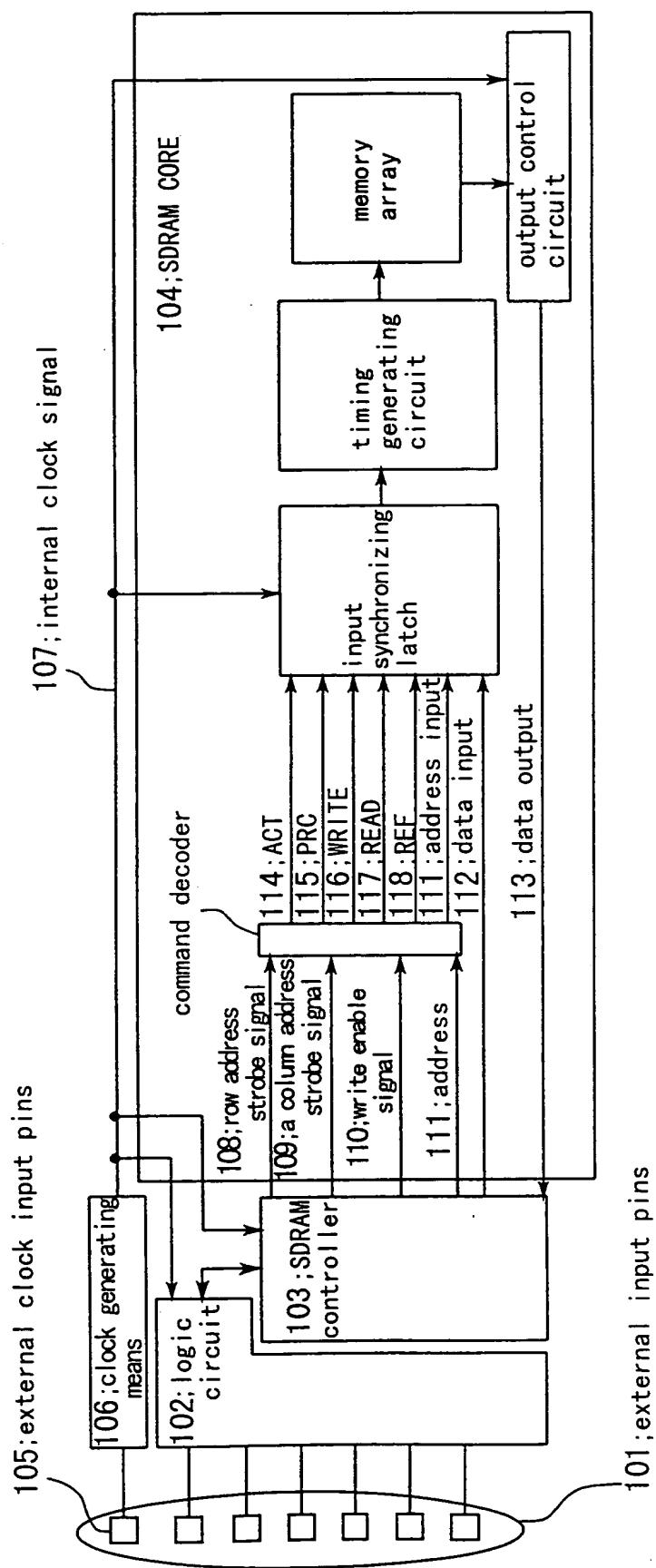




Fig. 12 Prior Art





*FIG. 13 Prior Art*

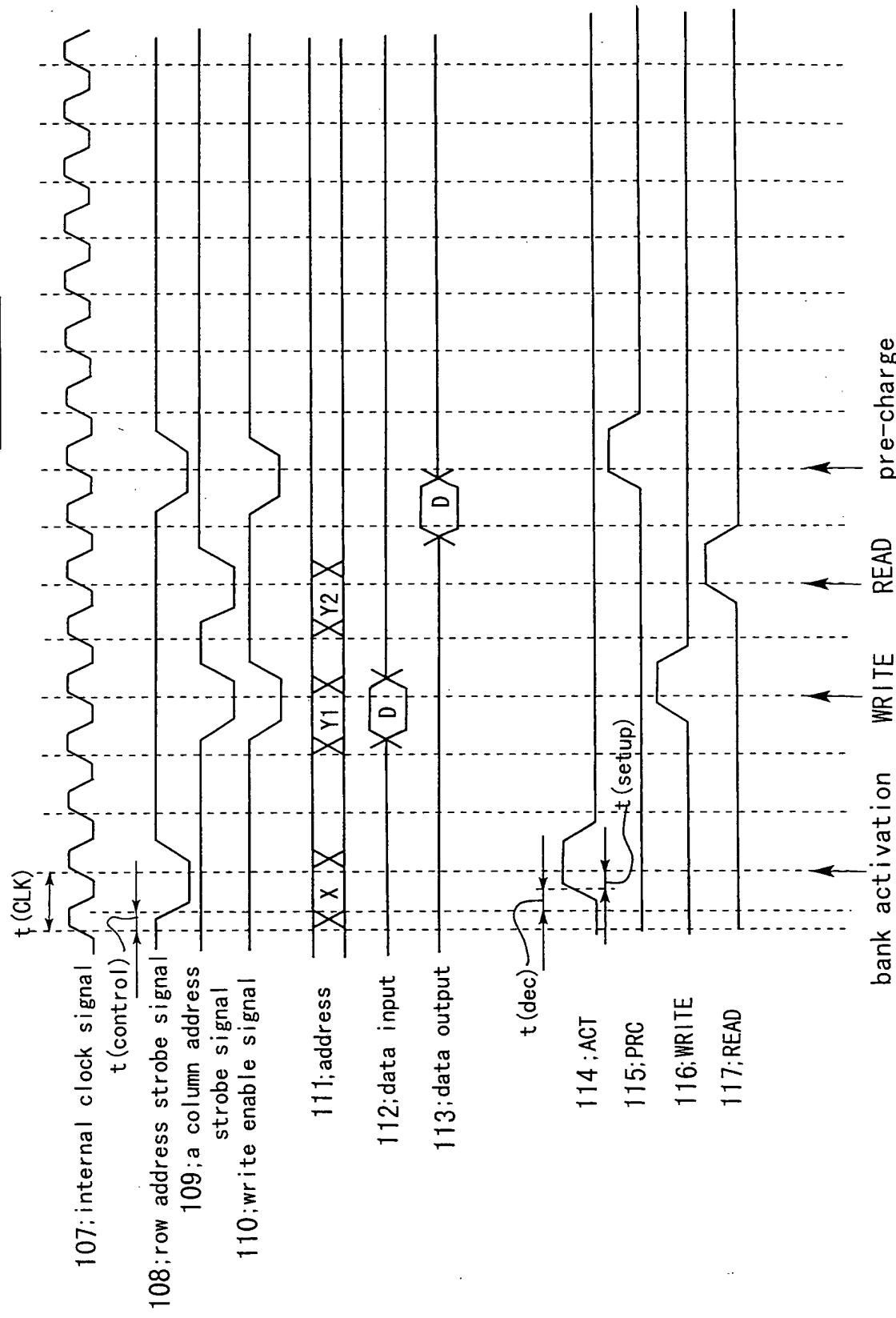
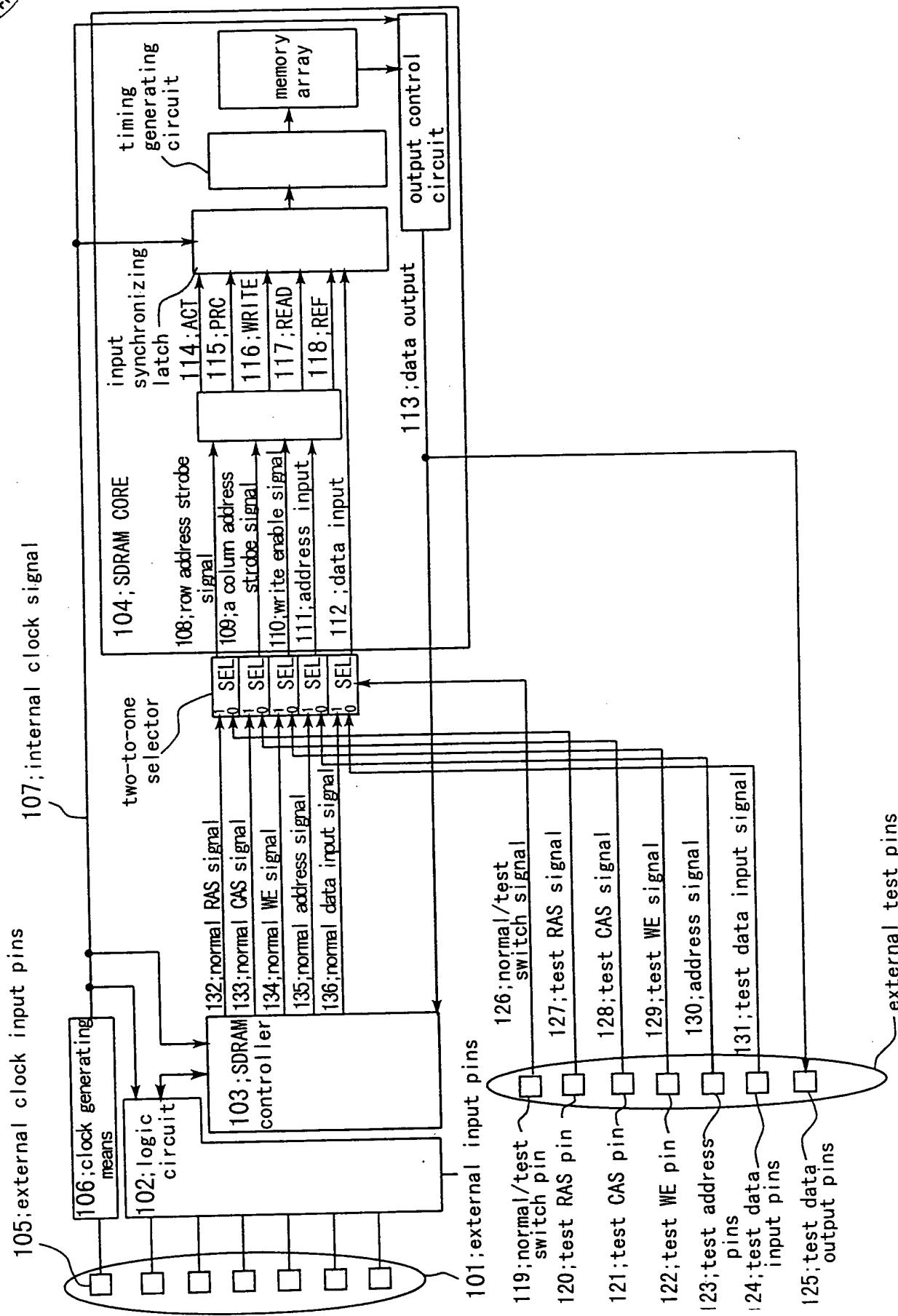




FIG. 14 Prior Art





## Prior Art

